CLAIMS

1. A decoder, having an input signal and a first output signal, comprising:

a multiplier for multiplying a predetermined value by the input signal to generate an intermediate signal, wherein the input signal has a pilot signal component and wherein the pilot signal component in the intermediate signal is a lower frequency than the pilot signal component in the input signal;

a filter for receiving the intermediate signal and for providing the pilot signal component as an output;

a phase lock loop for receiving the pilot signal component from the output of said filter, said phase lock loop determining an approximate phase of the pilot signal component of the input signal and generating at least one trigonometric function using the approximate phase of the pilot signal component of the intermediate signal;

means for using the at least one trigonometric function to phase align a first data component of the input signal and a second data component of the input signal and provide a phase aligned first data component; and

means for using the phase aligned first data component to generate the first output signal.

2. A decoder as in claim 1, wherein the at least one trigonometric function includes a sine function and a cosine function.

3. A decoder as in claim 1, wherein the predetermined value is retrieved from a table.

4. A decoder as in claim 3, wherein the predetermined value is a cosine value.

5. A decoder as in claim 1, wherein said decoder has a second output signal.

6. A decoder as in claim 5, wherein the first output signal is a right stereo channel and the second output signal is a left stereo channel, wherein the first data component is a difference between a left channel and a right channel, and wherein the second data component is a summation of the left channel and the right channel.

7. A decoder as in claim 1, wherein the means for using the phase aligned first data component to generate the first output signal comprises a stereo blender.

8. A decoder as in claim 7, wherein said stereo blender comprises:

a first filter for providing a first filter output;

a second filter for providing a second filter output; and

combining circuitry, coupled to said first filter and said second filter, said combining circuitry combining the first filter output and the second filter output to produce the first and second output signals.

9. A decoder as in claim 8, wherein filter coefficients of said first filter are selectable, and filter coefficients of said second filter are selectable.

10. A decoder as in claim 8, wherein said first filter and said second filter are FIR filters.

11. A decoder as in claim 1, wherein the decoder is used in a radio receiver.

12. A decoder as in claim 1, wherein the predetermined value is approximate to, but not equal to, a frequency of the pilot signal component in the input signal.

13. A decoder as in claim 12, wherein the predetermined value is within 3 kilohertz of the frequency of the pilot signal component in the input signal.

14. A decoder as in claim 1, further comprising:

a decimator, coupled between said filter and said phase lock loop.

15. A decoder as in claim 14, wherein said decimator reduces a frequency of the intermediate signal.

16. A decoder as in claim 15, wherein said decimator reduces the frequency of the intermediate signal by a factor of 20.

17. A decoder as in claim 1, wherein said phase lock loop operates at a frequency less than one tenth a frequency of the input signal.

18. A method for decoding an input signal using only digital circuitry, comprising:

receiving the input signal;

using a phase lock loop having feedback to estimate phase information of at least one component of the input signal using only digital circuitry, the phase lock loop receiving an intermediate signal having a phase value; and

completing decoding of the input signal to generated an output signal.

19. A method as in claim 18, wherein the step of using the phase lock loop further comprises:

adding a predetermined phase correction to the phase value to produce a resultant phase value, wherein the predetermined phase correction is a function of a delay of a portion of the digital circuitry.

20. A method as in claim 18, wherein the step of using the phase lock loop further comprises:

multiplying the resultant phase value by a predetermined positive integer to produce a multiplied resultant phase value; and

determining at least one trigonometric function of the multiplied resultant phase value.

21. A method for decoding an input signal containing information on a left channel L and a right channel R, the method comprising:

filtering a L+R signal to produce a filtered L+R signal, where L is the left channel and R is the right channel;

filtering a L-R signal to produce a filtered L-R signal; and

after filtering the L+R signal and the L-R signal, combining the filtered L+R signal and the filtered L-R signal to produce a left channel output signal and a right channel output signal.

22. A method as in claim 21, wherein said step of filtering the L+R signal and said step of filtering the L-R signal are performed using at least one FIR filter.

23. A method as in claim 21, wherein said step of filtering the L+R signal and said step of filtering the L-R signal are performed in software.

24. A method as in claim 23, further comprising:

providing software modifiable filter coefficients.